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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,215	03/25/2004	Mikiya Uchida	10873.1371US01	6568

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EXAMINER	
VU, HUNG K	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/809,215	UCHIDA ET AL.
	Examiner	Art Unit
	Hung Vu	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-13* is/are pending in the application.

4a) Of the above claim(s) *10-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/6/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The indicated allowability of claim 2 is withdrawn in view of the IDS submitted by Applicants to Yuzurihara (EP 1075028, of record) and Maeda (PN 6,492,668, of record). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yuzurihara (EP 1075028, of record) in view of Maeda (PN 6,492,668, of record).

Yuzurihara discloses, as shown in Figures 1-5, a solid-state imaging apparatus, comprising:

a plurality of photosensitive cells (1) disposed in a matrix in a photosensitive region on a semiconductor substrate (21,22);

a driving unit for driving the plurality of photosensitie cells,

wherein each of the photosensitive cells includes:

a photodiode (1) formed to be exposed on a surface of the semiconductor substrate, for accumulating signal charge obtained by subjecting incident light to photoelectric exchange;

a transfer transistor (2) formed on the semiconductor substrate, for transferring the signal charge accumulated in the photodiode;

a floating diffusion layer (15) formed on the semiconductor substrate, for temporarily accumulating the signal charge transferred by the transfer transistor;

an amplifier transistor (5) formed on the semiconductor substrate, for amplifying the signal charge temporarily accumulated in the floating diffusion layer,

wherein a source/drain diffusion layer (5) provided in the amplifier transistor is covered with a salicide layer (30);

the floating diffusion layer is formed to be exposed on the surface of the semiconductor substrate.

Yuzurihara does not disclose the impurity concentration of the floating diffusion layer is lower than an impurity concentration of the source/drain diffusion layer of the amplifier transistor. However, Maeda discloses a solid-state imaging apparatus comprising a transistor having an impurity concentration of a floating diffusion layer (FD) is lower than an impurity concentration of a source/drain diffusion layer (4b) of an amplifier transistor. Note Figures 6 and 12 of Maeda. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the impurity concentration of the floating diffusion layer of Yuzurihara being lower than an impurity concentration of the source/drain diffusion layer of the amplifier transistor, such as taught by Maeda in order to reduce the leakage current of the device.

Regarding claims 3 and 7, Yuzurihara and Maeda disclose the invention substantially as claimed including the apparatus as recited in the rejection above. Yuzurihara and Maeda further disclose each of the photosensitive cells further includes a reset transistor for resetting the floating diffusion layer, the driving unit includes: a vertical driver circuit for simultaneously driving the

transfer transistor and the reset transistor in a vertical direction and a horizontal driver circuit for outputting a signal. Yuzurihara and Maeda do not disclose the noise suppressing circuit. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Yuzurihara and Maeda comprising the noise suppressing circuit in order to reduce the noise generating in the circuit and to improve the circuit performance.

Regarding claims 4 and 8, Yuzurihara and Maeda disclose the invention substantially as claimed including the apparatus as recited in the rejection above. Yuzurihara and Maeda do not disclose the source/drain diffusion layer provided in the plurality of transistors constituting the vertical driver circuit and the horizontal driver circuit is covered with a salicide layer. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the source/drain diffusion layer of Yuzurihara and Maeda covering with a salicide layer in order to reduce contact resistivity.

Regarding claim 5, Yuzurihara and Maeda disclose the transfer transistor and the amplifier transistor are composed of an n-type MOS transistor.

Regarding claim 6, Yuzurihara and Maeda disclose the invention substantially as claimed including the apparatus as recited in the rejection above. Yuzurihara and Maeda do not disclose the vertical driver circuit and the horizontal driver circuit are composed of a dynamic logic circuit. However, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to form the device of Yuzurihara and Maeda composing of a dynamic logic circuit in order to perform the desired function.

Regarding claim 9, Yuzurihara and Maeda disclose the impurity concentration of the floating diffusion layer is $1x10^{18}$ cm^{-3} or less.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung Vu whose telephone number is (571) 272-1666. The examiner can normally be reached on Tuesday to Friday 6:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272 - 1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vu

March 1, 2006

Hung Vu

Primary Examiner